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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,941	03/11/2004	Abdallah Bacha	068758.0177	4868

31625 7590 11/28/2006

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,941	BACHA ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 9/19/2006.

2. Claims 1, 8, 14 have been amended, no new claims have been added and no claims have been canceled. Thus, Claims 1-21 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3/11/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is considered by the examiner.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy filed on 6/10/2004 has been received.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuzaki (US Patent Application Publication 2001/0050856).

For claim 1, Matsuzaki teaches the following limitations:

A circuit module (14 in Fig 7) comprising: a circuit board (160); multiple circuit units on the circuit board (120-127); at least one clock input on the circuit board for receiving an external clock signal (CLK in Fig 7); a first phase locked loop (PLL) unit (15) on the circuit board for providing an internal clock signal (23) based on the external clock signal (CLK) to a first set of at least one of the circuit units (120, 121); and a second PLL unit (16) on the circuit board for providing an internal clock signal (25) based on the external clock signal (CLK) to a second set of at least one of the circuit units (126, 127), wherein the second set and the first set are mutually exclusive (first set with 120 and 121, and second set with 126,127 are mutually exclusive, since the two sets do not share any common module as shown in Figure 7).

For claims 2-4, circuit module is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4, Fig 8) on the circuit board and also the same clock input on the circuit board (CLK, Fig 7).

For claim 5, 22 is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 6 and 7, feedback loops are shared by two PLLs (21) and the feedback loops have input to both PLL. 25 and 23 of Fig 7 are the two branches of feedback loop.

For claim 8, Matsuzaki teaches the following limitations:

A memory module (14 in Fig 7) comprising: a circuit board (160); multiple circuit units on the circuit board (120-127); at least one clock input on the circuit board for receiving an external clock signal (CLK in Fig 7); a first phase locked loop (PLL) unit (15) on the circuit board for providing an internal clock signal (23) based on the external clock signal (CLK) to a first set of at least one of the circuit units (120, 121); and a second PLL unit (16) on the circuit board for providing an internal clock signal (25) based on the external clock signal (CLK) to a second set of at least one of the circuit units (126, 127), wherein the second set and the first set are mutually exclusive (first set with 120 and 121, and second set with 126,127 are mutually exclusive, since the two sets do not share any common module).

For claims 9-10, circuit module is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4 in Fig 14) on the circuit board and also the same clock input (CLK, Fig 14) on the circuit board.

For claim 11, 22 is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 12 and 13, feedback loops are shared by two PLLs (21) and the feedback loops have input to both PLL (Fig 14). 25 and 23 of Fig 7 are the two branches of feedback loop.

For claim 14, Matsuzaki teaches the following limitations:

A circuit module (14 in Fig 7) comprising: a circuit board (160); a plurality of memory chips arranged along the width of the circuit board (120-127) comprising a first set of memory chips (120-123) and a second set of memory chips (124-127); at least one clock input on the circuit board for receiving an external clock signal ("CLK" in Fig 7); a first phase locked loop (PLL) unit (16) arranged within the first set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (120, 121); and a second PLL unit (15) arranged within said second set of memory chips for providing an internal clock signal based on the external clock signal to at least one of the memory chips (126, 127), wherein the second set and the first set are mutually exclusive (first set with 120 and 121, and second set with 126,127 are mutually exclusive, since the two sets do not share any common module).

For claims 15 and 16, PLLs are approximately at the center.

For claims 17-18, circuit module is a memory module and units are memory chips ([0077]). PLL units have clock inputs that are connected to different clock inputs (CLK4

in Fig 14) on the circuit board and also the same clock input (CLK, Fig 14) on the circuit board.

For claim 19, 22 is the feedback loop for PLL1 and PLL2-25-p3-p2-PLL2 is the feedback loop for PLL2. Frequency of CLK2 is controlled by comparing CLK4 with CLK and CLK4 is transmitted over feedback loop (Fig 8, [0051]).

For claims 20 and 21, feedback loops are shared by two PLLs (21) and the feedback loops have input to both PLL (Fig 14). 25 and 23 of Fig 7 are the two branches of feedback loop.

Response to Arguments

Applicant's arguments filed on 9/19/06 have been fully considered but they are not persuasive.

Applicant argues that Matsuzaki does not anticipate the claimed invention as the two PLLs of Matsuzaki provide clock signal to all memory chips.

Examiner disagrees. Examiner agrees that the two PLLs (15, 16) of Matsuzaki provide clock signal to all memory chips (120-127; Fig 7). However, claim does not prohibit providing clock signals from two PLLs to all memory chips. Claim requires first PLL (15) to provide clock to a first set comprising at least one chip (120, 121) and second PLL

(16) to provide clock to a second set comprising at least one chip (126, 127), wherein first and second sets are mutually exclusive (120-121 is different from 126-127). Claim does not require that first set be independent of second PLL and second set be independent of first PLL.

Applicant further argues that Matsuzaki's approach is quite different from applicant's approach of providing internal signal to a first and second number of circuit units. Therefore, Matsuzaki does not anticipate the claimed invention.

Examiner disagrees. As long as claim language does not reflect the difference between prior art and applicant's invention, such argument is invalid. Therefore, Matsuzaki is the proper basis of 102(b) rejection for the claimed invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the

statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/24/06